## REMARKS

In response to the Final Office Action mailed July 23, 2009, Applicants respectfully request reconsideration. Claims 1 and 3-30 were previously pending in this application. By this amendment, claims 1, 24, and 26 have been amended. As a result, claims 1 and 3-30 are pending for examination with claims 1, 24, 26, and 30 being independent. No new matter has been added.

### Rejections Under 35 U.S.C. §103 based on Lewis, George and Horning

The Office Action rejected claims 1 and 3-25 (including independent claims 1 and 24) under 35 U.S.C. §103(a) as being allegedly unpatentable over Lewis et al., U.S. Patent No. 5,797,043 ("Lewis") in view of George, U.S. Patent No. 6,785,829 ("George") and further in view of Horning et al., U.S. Patent No. 5,420,998 ("Horning"). Applicants respectfully disagree.

A. Independent Claim 1

The cited references do not teach or suggest all of the limitations of claim 1.

In particular, none of the cited references teaches or suggests that the stream register unit is configured to:

> "in response to a request for a data item from the execution unit, when the data item in located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit,
>
> *when the at least one stream register unit FIFO does not contain the data item in the next location,*
>
> *request the data item from the FIFO coupled to the peripheral by setting a "taken" signal across the communication path to a logic high, and*
>
> *when the FIFO coupled to the peripheral indicates that the data item is not available at the FIFO coupled to the peripheral by sending a "valid" signal set to a logic low, send a stall signal to the execution unit causing the execution unit to stop executing instructions,*"

as recited, *inter alia*, in amended claim 1 (emphasis added).

Support for the amendments to claim 1 can be found at least on page 4, lines 19 – page 5, lines 1-5 of Applicants' specification.

On pages 2-4, the Office Action alleges that Lewis and George teach some limitations of claim 1. Applicants respectfully disagree.

Furthermore, on page 4, the Office Action concedes that the combination of Lewis and George "fails to teach system wherein the stream register unit is arranged to, if the signal sent by the FIFO is the said different signal indicating that the data is not available, send a stall signal to the processor, causing the processor to stop executing instructions." Applicants respectfully note that claim 1 contains **different** language and recites, *inter alia*, that "the stream register unit is configured to: ... when the at least one stream register unit FIFO does not contain the data item in the next location, request the data item from the FIFO coupled to the peripheral by setting a "taken" signal across the communication path to a logic high, and when the FIFO coupled to the peripheral indicates that the data item is not available at the FIFO coupled to the peripheral by sending a "valid" signal set to a logic low, send a stall signal to the execution unit causing the execution unit to stop executing instructions."

The Office Action then alleges that Horning "teaches a system wherein a processing unit is configured to, **when the processing unit does not contain** the data item in the next location, request the data item from the memory coupled to the peripheral, and send a stall signal to the execution unit, causing the execution unit to stop executing instructions (column 11, lines 5-15, when the predetermined level is at empty is considered the point at which the next data item is not available and the system issues a request from the source which is analogous to the peripheral and halts the data transfer which is considered the stall signal which stops the execution of the transfer function)" (emphasis added). Applicants respectfully note that claim 1 recites when ***the at least one stream register unit FIFO*** does not contain the data item in the next location ... (emphasis added).

Applicants respectfully submit that, contrary to the assertions made in the Office Action, Horning does not teach or suggest "the stream register unit is configured to: ... when the at least one stream register unit FIFO does not contain the data item in the next location, request the data item from the FIFO coupled to the peripheral and send a stall signal to the execution unit causing the execution unit to stop executing instructions."

Horning describes a dual disk drive **peripheral data storage system** (Horning, Abstract) (emphasis added). Thus, throughout the reference, with respect to the term "peripheral," Horning describes peripheral data storage system. In Horning, the dual disk drive is a combination of a hard disk drive and a solid state disk drive (Horning, Abstract).

The cited portion belongs to a description of Horning's Figs. 4A-4C that present a flowchart illustrating the steps involved in writing data **to the dual disk drive 10** (Horning, col. 10, lines 13-14) (emphasis added). Thus, in the cited portion, Horning describes how the data is written **to** the **peripheral** dual disk drive. Therefore, contrary to the assertions made on page 4 of the Office Action, "the source" of Horning is not "analogous to the peripheral." Indeed, Horning describes "the source data transfer component, i.e. **the host interface** 26" (Horning, col. 11, lines 13-15) (emphasis added).

Furthermore, in the cited portion, Horning states that if the amount of data in the transfer buffer falls below a predetermined level (and there is more data to be transferred), then the buffer controller 34 **halts data transfer to the target data transfer component**, i.e., the cache/SSD data transfer unit 46 in this case, and requests **the next data items from the source data transfer component**, i.e., the host interface 26 in this case (Horning, col. 11, lines 8-15) (emphasis added). Thus, Horning does not state that "when the predetermined level is at empty is considered the point at which the next data item is not available." Indeed, Horning only states "if the amount of data in the transfer buffer falls below a predetermined level... ." Nowhere does the reference even mention that "the predetermined level is at empty," as stated in the Office Action. Moreover, on the contrary, Horning states that the buffer controller 34 attempts to keep the transfer buffer **at least partially full** during the data transfer (Horning, col. 11, lines 6-8) (emphasis added).

Furthermore, in Horning, if the amount of data in the transfer buffer falls below a predetermined level, then the buffer controller 34 **halts data transfer to the target data transfer component**, i.e., the cache/SSD data transfer unit 46 (Horning, col. 11, lines 8-12) (emphasis added). Thus, Horning describes that data transfer to the cache/SSD data transfer unit is halted. In contrast, claim 1 recites that the stream register unit is configured to:... send a stall signal ***to the execution unit*** causing the execution unit to ***stop executing instructions*** (emphasis added). Thus, as would be understood by one of skill in the art, **halting the data transfer** to the cache/SSD data transfer unit of Horning is different from sending "a stall signal to the execution unit causing the execution unit to stop executing instructions," as recited in claim 1. In addition, Horning states that **unless an error** condition arises **the processor** 30 **is not involved** in the data transfer beyond commencing the transfer (Horning, col. 11, lines 1-3) (emphasis added). Thus, Horning does not teach or suggest that the stream register unit is configured to:... send a stall

signal to the execution unit causing the execution unit to stop executing instructions, as recited in claim 1.

In addition, while claim 1 recites that the stream register unit is configured to: ... when the at least one stream register unit FIFO ***does not contain the data item*** in the next location, ***request the data item*** from the FIFO coupled to the peripheral ... ," Horning states that if the amount of data in the transfer buffer falls below a predetermined level then the buffer controller 34 ... requests **the next** data items from the source data transfer component (emphasis added). Thus, in Horning, the next data items are requested rather than the same data item that is not contained in the next location in the at least one stream register unit FIFO.

Moreover, as discussed above, claim 1 has been amended to recite, *inter alia*, "when the at least one stream register unit FIFO does not contain the data item in the next location, ***request the data item from the FIFO coupled to the peripheral by setting a "taken" signal across the communication path to a logic high, and when the FIFO coupled to the peripheral indicates that the data item is not available at the FIFO coupled to the peripheral by sending a "valid" signal set to a logic low***, send a stall signal to the execution unit causing the execution unit to stop executing instructions" (emphasis added). None of the cited references teaches or suggests the above limitations of claim 1.

In view of the foregoing, claim 1 patentably distinguishes over Lewis, George and Horning, either alone or in combination, and is in condition for allowance.

Claims 3-23 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 1 and 3-23 is respectfully requested.

B. Independent Claim 24

The cited references do not teach or suggest all of the limitations of claim 24.

On pages 3-5, the Office Action appears to reject claim 24 for the same reasons as those used to reject claim 1.

Claim 24 has been amended to recite, *inter alia*, that the stream register is configured to:

> in response to a request for a data item from the execution unit, when the data item in located in a next location of the at least one stream register unit FIFO, provide the data item to the execution unit, and
>
> *when the at least one stream register unit FIFO does not contain the data item in the next location,*

*request the data item from the FIFO coupled to the peripheral by setting a "taken" signal across the communication path to a logic high, and*

*when the FIFO coupled to the peripheral indicates that the data item is not available at the FIFO coupled to the peripheral by sending a "valid" signal set to a logic low, send a stall signal to the execution unit causing the execution unit to stop executing instructions.*

(Emphasis added).

Support for the amendments to claim 24 can be found at least on page 4, lines 19 – page 5, lines 1-5 of Applicants' specification.

As should be clear from the above discussion, none of the cited references teaches or suggests the above limitations of claim 24.

In view of the foregoing, claim 24 patentably distinguishes over Lewis, George and Horning, either alone or in combination, and is in condition for allowance.

Claim 25 depends from claim 24 and is allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 24 and 25 is respectfully requested.

Rejections Under 35 U.S.C. §103 based on Lewis and Garcia

The Office Action rejected claims 26-30 (including independent claims 26 and 30) under 35 U.S.C. 103(a) as allegedly being unpatentable over Lewis in view of Garcia et al., U.S. Patent No. 6,433,785 ("Garcia"). Applicants respectfully disagree.

A. Independent Claim 26

Claim 26, as amended, recites, *inter alia*, that the stream register is arranged to: ...***when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor***; send the request to the peripheral by setting a "taken" signal across a communication path between the peripheral and the at least one FIFO to a logic high and receive one or more signals back from the peripheral indicating availability of the requested data item, when the data item is available, send the data item to the processor, and ***when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request*** (emphasis added).

Applicants respectfully reiterate that the Office Action **does not address** the highlighted limitations of claim 30, as has been previously indicated in Applicants' response to an Office Action mailed December 15, 2008. Moreover, claim 26 has been amended to recite, *inter alia*, "send the request to the peripheral ***by setting a "taken" signal across a communication path between the peripheral and the at least one FIFO to a logic high***" (emphasis added). Support for the amendment to claim 26 can be found at least on page 4, lines 19-26 of Applicants' specification. None of the cited references teaches or suggests this limitation of claim 26.

In addition, while, on page 11, the Office Action states that Lewis **teaches** a stream register being part of a processor, on page 3, the Office Action concedes that Lewis **fails to teach** a system wherein a stream register unit being part of the processor. These statements appear to be contradictory.

Furthermore, as should be clear from the above discussion, the cited references do not teach or suggest the stream register is arranged to: ... ***when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request***, as recited in claim 26 (emphasis added).

In view of the foregoing, claim 26 patentably distinguishes over Lewis and Garcia, either alone or in combination, and is in condition for allowance.

Claims 27-29 depend from claim 26 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection of claims 26-29 is respectfully requested.

B. Independent Claim 30

Claim 30 recites, *inter alia*, that the stream register is arranged to: ... ***when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor***; and send the request to the memory and receive one or more signals back from the memory indicating availability of the requested data item, and, when the data item is available, send the data item to the execution unit of the processor, and, ***when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request*** (emphasis added). Applicants respectfully reiterate that the Office Action **does not address** the highlighted limitations of claim 30, as has

been previously indicated in Applicants' response to an Office Action mailed December 15, 2008.

I n addition, while, on page 11, the Office Action states that Lewis **teaches** a stream register being part of a processor, on page 3, the Office Action concedes that Lewis **fails to teach** a system wherein a stream register unit being part of the processor. These statements appear to be contradictory.

Furthermore, as should be clear from the above discussion, the cited references do not teach or suggest that the stream register is arranged to: ... ***when the requested data item is not in the at least one FIFO, send a stall signal to the execution unit of the processor***; and,... ***when the data item is not available and when the stall signal has been active for a predetermined amount of time, send a timeout signal to the execution unit of the processor causing the processor to interrupt such that it can execute tasks other than the request*** as recited in claim 30 (emphasis added).

In view of the foregoing, claim 30 patentably distinguishes over Lewis and Garcia, either alone or in combination, and is in condition for allowance.

Accordingly, withdrawal of the rejection of claim 30 is respectfully requested.

## CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' representative at the telephone number indicated below to discuss any outstanding issues relating to the allowability of the application.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825 under Docket No. S1022.81044US00 from which the undersigned is authorized to draw.

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Respectfully submitted,

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